Masaki Morita Master's Student https://masaki42482.github.io/

Education

Graduate School of Information Science and Technology,
The University of Tokyo Tokyo, Japan
M.S. in Information Physics and Computing Apr 2024 - Mar 2026 *(expected)*

- Supervisor: Prof. Hiroshi Nakamura
- Advisor: Assoc. Prof. Hideki Takase
- Research area: Hardware Security and Computer Architecture

Faculty of Engineering, The University of Tokyo Tokyo, Japan
B.E. in Mathematical Engineering and Information Physics Apr 2020 - Mar 2024

- Undergraduation Thesis
  "Differential Circular Polarization Measurement for Detecting Human Sweat Gland Response to Sub-Terahertz Waves"
  - Supervisor: Assoc. Prof. Yasuaki Monnai
  - Research area: Terahertz Wave Technology and Biomedical Engineering

Publications and Presentations

Paper | Peer Reviewed

1. Takuya Kojima, **Masaki Morita**, Hideki Takase and Hiroshi Nakamura, "An Open-Source Framework for Efficient Side-Channel Analysis on Cryptographic Implementations", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, doi: 10.1109/TCAD.2026.3654878

Japanese Domestic Conferences | Non-Peer Reviewed

1. **Masaki Morita**, Takuya Kojima, Haruto Ishii, Hideki Takase, and Hiroshi Nakamura, "Optimizing Deep Learning Based Side-Channel Attacks Methods by Preprocessing Based on Autoencoder" *Technical Report (HWS)*, Naha, Okinawa, March 2025.
2. **Masaki Morita**, Takuya Kojima, Hideki Takase, and Hiroshi Nakamura, "An Autoencorder-based Compression for a faster DL-SCA", *Cross-Disciplinary workshop on computing Systems, Infrastructures, and programming(xSIG)*, Takamatsu, Kagawa, August 2025 (Poster)

International Conferences | Peer Reviewed

1. **Masaki Morita**, Takuya Kojima, Haruto Ishii, Hideki Takase and Hiroshi Nakamura, "A Data Compression Method for DL-SCAs using Denoising Autoencoders", *IEEE Symposium on Low-Power and High-Speed Chips and Systems (COOL Chips 28)*, Tokyo, Japan, April 2025. (Poster)
2. **Masaki Morita**, Takuya Kojima, Haruto Ishii, Hideki Takase and Hiroshi Nakamura, "A Denoising Preprocess Method for Side-Channel Attacks Using Autoencoders", *2025 IEEE International Symposium on Hardware Oriented Security and Trust (HOST)*, San Jose, United States of America, May 2025. (Presentation and Demonstration)

Awards and Honors

- **Featured Poster Award**, COOL Chips 28, April 2025

Scholarships

Funai Overseas Scholarship | Sep 2026 - Aug 2028

- 2 years scholarship for Ph.D study abroad provided by **Funai Foundation for Information Technology**
- Tuition: Up to 14,000 USD/year
- Medical insurance: Full coverage
- Living expenses: Up to 36,000 USD/year

Fulbright Scholarship | Sep 2026 - Aug 2028

- Designated as a principal candidate for a 2026 Fulbright grant
- 1 years scholarship for Ph.D study abroad provided by **Japan-United States Educational Commission (JUSEC)**
- Declined due to non-concurrent funding policy.

Professional Experiences

Teaching Assistant, The University of Tokyo | Tokyo, Japan Apr 2024 - Present

- Assisted in the lab course "Introduction of Digital Circuits" for undergraduate students.
- Instructed students on the use of FPGA boards and programming in VHDL.
- Provided support in debugging and troubleshooting digital circuit designs.

ookami Co., Ltd. | Tokyo, Japan Jul 2024 - Dec 2024

- Designed and implemented APIs and managed backend data systems
- Collaborated with front-end developers to integrate user-facing elements with server-side logic.
- Proposed and discussed feature ideas in team meetings to improve product functionality and user experience.
- Led and coordinated work among fellow interns to streamline development and ensure timely delivery.